Hardware Testing and Implementation of RapidIO Protocol on the ISAAC iBoard for use in the NEXUS Testbed

Carson Umsted

Section 345 – Flight System Avionics
Jet Propulsion Laboratory
California Institute of Technology

March 3, 2011

This Cooperative Education Report has been submitted to Dr. Yutao He and has been approved for release and submission to Dr. Francis X. Flores, Cooperative Education Director, Cal Poly, Pomona **during the 9th week of the quarter.**

Signed _____ Dated_____

Table of Contents

Objectives

The objective was to fully test the functionality of new ISAAC iBoards coming from the manufacturer and then begin implementation of the RapidIO Protocol to the new iBoard to be used in the NEXUS Testbed. In order to meet this goal, I had to complete the following:

1. Verify correct operation of necessary board peripherals by running extensive testing on unverified components, troubleshooting and correct any issues found in the verification process.
2. Research RapidIO Protocol and investigate the work done by others on other FPGA boards.
3. Begin configuring the core by following the iBoard features and specifications, then test the functionality of the core using loopback and point-to-poing methods.

Executive Summary

I am assisting the NEXUS (NEXtbUS) and ISAAC (Instrument ShAred Artifact for Computing) teams in achieving a highly reusable, highly configurable FPGA (Field Programmable Gate Array) system which uses a unified, high-speed bus standard. One of my tasks is to verify that all new ISAAC iBoards' features are functioning as expected by using my previous builds to test these features and resolving any errors found. My other task is to investigate and implement the RapidIO protocol and to implement it onto the new ISAAC iBoards to be used in the NEXUS testbed. Completing these tasks will demonstrate the potential of both NEXUS and ISAAC technology. This will allow others to see the power in making use of a unified, modular system.

Description of the Co-op Position and Activities

Jet Propulsion Laboratory (JPL) is a NASA field center managed by the California Institute of Technology which engages in both a wide variety of research and development and flight projects, concentrating on advancing technology to improve the lives of people here on Earth.

NEXUS (NEXtBUs) is a research project which goal is to implement a scalable interconnect networking technology for future spacecraft avionics systems. [2] Instrument ShAred Artifact for Computing (ISAAC) is a research and technology development project at JPL focused on improving upon the current method of hardware and software development. [1] The six components of ISAAC, shown in Figure 1, each play an important role in the achievement of ISAAC's goal. iBoard is the target hardware used for the implementation of my developed systems for performance evaluation.

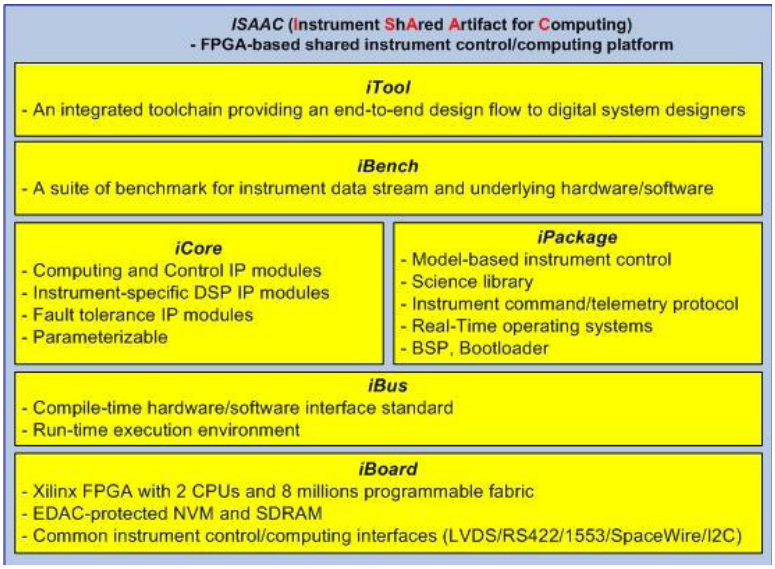

Figure 1: Components of ISAAC

iBoard, the chosen target hardware for demonstrating NEXUS technology, has one Virtex-5 FPGA with two embedded PowerPC 440 processors. In addition to these features which provide a high level of performance, the iBoard has many other key features which enable it to meet the requirements of many different projects with the capability of having a path to flight. This technology meets the requirements of and provides NEXUS with the hardware it needs to exhibit its scalable interconnects. By having modular, path-to-flight hardware to show the research of NEXUS, the validity of the ideas are further reinforced because it has been proven on typical hardware similar to that which will be used in future flight missions.

Prior to this co-op position I had worked with my mentor in testing the first few iBoards of the current version. As a team, a suite of feature test build applications were built and tested

on known working hardware and used as the baseline configuration for testing of the iBoard. At the end of the previous work period, I had tested the first two boards, but 8 more remained at the start of this quarter.

For the 5 weeks, I assisted in testing the functionality of the aforementioned 8 new iBoards by performing the power-up procedure and using the different test builds and observing the results.

The following few weeks were spent researching RapidIO protocol and previous implementations on other FPGA devices. This included running the network testbed with development boards and replicating procedures developed by previous research.

The final weeks have been used to begin the implementation of RapidIO on the actual ISAAC hardware and verify its operation to be that of the development boards used earlier in the work period.

Descriptions of Project(s) Completed and Data

As with the previous co-op period in the fall quarter, there was a strict procedure that must be followed to ensure that the board would be safe to power on. Before doing any programming of and powered testing, the board had to be visually inspected and probed with a multi-meter for power supply voltage faults. If the test procedure was not followed as written, when the board was powered up, most if not all of the board components would be ruined because of over-current conditions.

Unlike the first 2 boards, there were shorts found on the board due to bridging of the some of the capacitors. Normally, this would be a quick resolution, however, the possible bridged connections could only be narrowed to a possible twenty capacitors and the parts were

less than 3 millimeters in size. This made a visual identification difficult so individual inspection by the use of a microscope was necessary. I spent time looking through the microscope to see where solder has flowed across the capacitor pads and then using the soldering iron to remove the excess solder. In some cases, it was necessary to remove the part and then clean the board because the excess solder was directly under the part. Much time was spent simply resolving these issues on the boards with the capacitors since there were so many on the board that were shorted.

After investigation into the why these problems occurred, it was found that the footprint for the capacitors were closer together than they needed to be. Although they weren't off by more than a few mils, it was very critical because of the miniaturized circuit components. Future revisions are set to use the correct footprint to prevent any further issues with this.

In addition to shorted capacitors, there were some minor problems with the connections between the voltage regulators and the iBoard. I resolved these issued by resoldering the chips to the board. The board was not able to be powered up.

With the board powered on, I used the test builds to test the board features such as SRAM (Static Random Access Memory), UART (Universal Asynchronous Receiver/Transmitter), and DDR (Double Data Rate) memory. There were individual errors found with some of the tests, but were quickly resolved by looking at the board and identifying areas where a signal problem was. Once isolated, I was able to resolder the connections and verify the fix.

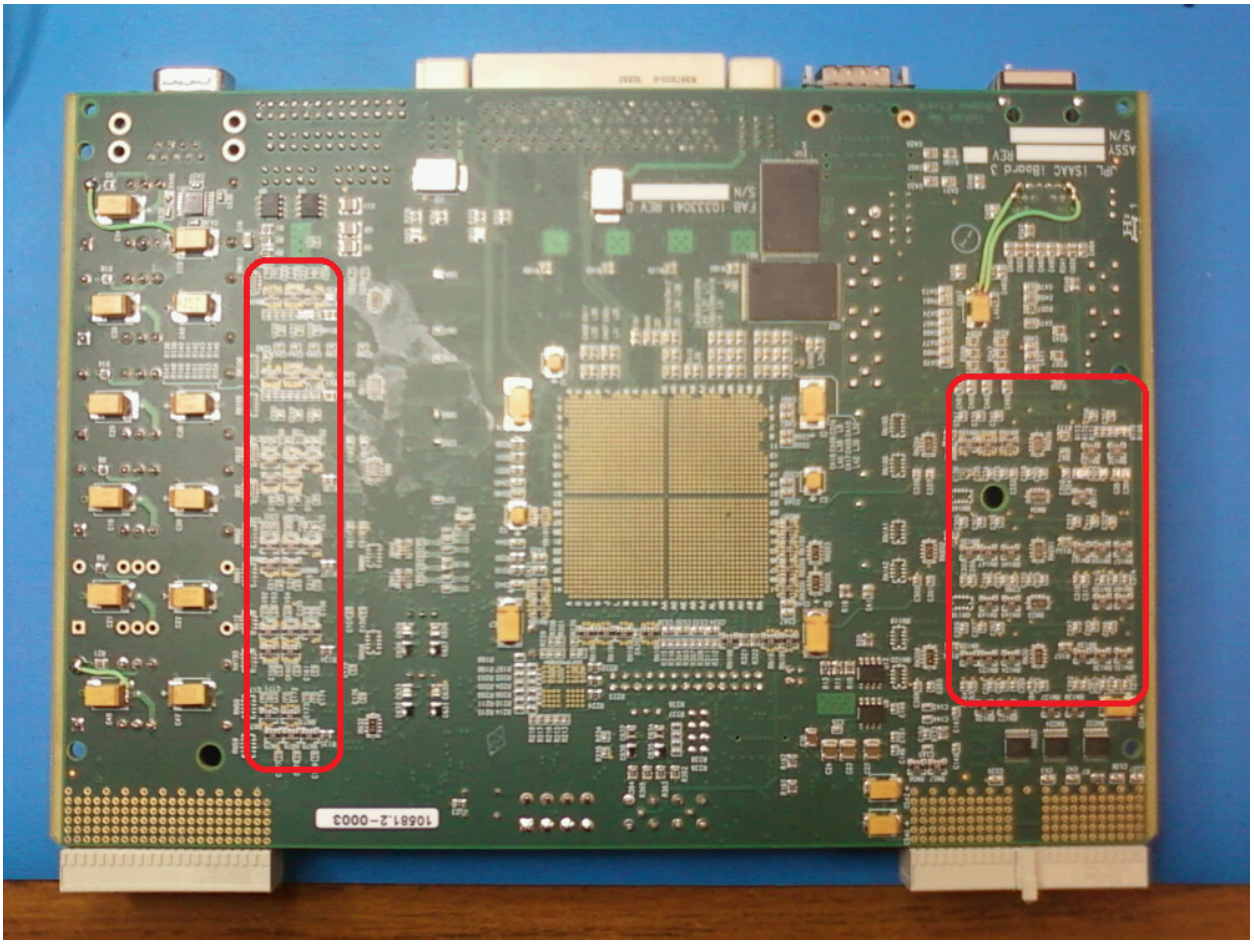

Figure 2: Bottom View of iBoard Showing 1 Area of capacitors

Once all boards had been tested, I moved on to researching RapidIO. Working through the documentation that other engineers had written based on ML-505 development boards, I re-implemented and verified the operation of the RapidIO physical and logical layers by successfully sending packets of data to the boards across a network and also using loopback methods.

Once I became familiar with the operation of the NEXUS Testbed, I began to implement the design onto iBoard. However, this was not as easy as with the development boards. The creation of the project is identical with the minor changes of specifying the correct FPGA device,

but running the design in hardware has proven unsuccessful at this time. The problem has been narrowed down to the reference clock which is connected to one internal block (tile) is not being properly forwarded to another tile which the external connectors are at. Reading through the documentation provided by Xilinx, the clock can be routed to a tile up to 3 away from another. The iBoard design has the two tiles adjacent to each other so there are no issues because of the design. [3] I have implemented some debug LED's on the board so I can verify visually the status of the connection and I see that the core is ready but does not have a clk.

This issue is ongoing and still being investigated. The short term solution to this would be to simply provide an external differential clock to the board and then verify the operation. I have spoken with other colleagues and have attempted many suggested solutions but as of now, there hasn't been anything that has been the root cause of the issue.

Note: Due to the sensitivity of technology development at JPL, I am unable to elaborate further on procedural details regarding my work.

Suggestions for Further Work, New Objectives, and Action Required

As research continues, I will continue my analysis of the issues that the iBoard's clock routing issues that has been recurring. When this is resolved, I would like to fully implement the NEXUS testbed and have real sources of data coming into iBoard and verify that the bus is still meeting the requirements set forth by NEXUS.

Personal Comments, Opinions, and Observations

As mentioned in my first report, this internship has been highly beneficial to me in both the academic and professional sense. I have become much more familiar with the testing process that is standard for new hardware. Having this opportunity has enable me to expand upon my professional networking skills. I have been more involved with weekly meetings where I can help talk out current technical issues with other works and hold discussion to find a solution.

Acknowledgement

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Research Apprenticeship Co-op Program, California State Polytechnic University, Pomona and the National Aeronautics and Space Administration.

References

[1] Y. He, C. Le, J. Zheng, K. Nguyen, and D. Bekker, "ISAAC – A case of highly-reusable, highly-capable computing and control platform for radar applications," *2009 IEEE Radar Conf.*, Pasadena, CA, May 2009.

[2] Y. He "NEXUS: A Network Testbed for Future Spacecraft Interconnects" Spring 2010. Student Independent Research Internship Announcement of Opportunity http://siri.jpl.nasa.gov/index.cfm?fuseaction=home.oppannounce&submenu=Student&semester=Spring%202010&CFID=4387&CFTOKEN=10080343

[3] Xilinx "Virtex-5 FPGA RocketIO GTX Transceiver User Guide" Oct. 30, 2009, http://www.xilinx.com/support/documentation/user_guides/ug198.pdf